In the claims:

In the final Office action, claims 5-9, 11-18 and 20-25 were pending.

Claims 5-9, 12-18 and 22-25 were allowed.

Claims 11, 20 and 21 were rejected.

Please cancel non-allowed claims 11, 20 and 21.

Please add new claim 26.

Please amend as follows:

1. (withdrawn) A method for manufacturing a block alterable memory cell, such method comprises the following steps:

depositing a screen oxide over a substrate layer;

depositing a mask implant layer over the screen oxide layer;

implanting memory cells in the portion of the substrate layer not covered by the mask implant layer;

etching a screen oxide and an initial gate oxide from memory cells;

depositing tunnel window mask;

etching a tunnel oxide layer;

depositing control poly layer; and

implanting source and drain regions.

2. (withdrawn) The method for manufacturing a block alterable memory cell of claim 1, wherein the step of deposing a control poly layer further comprising:

depositing a first oxide layer;

depositing an inter poly layer;

depositing a second oxide layer.

3. (withdrawn) The method for manufacturing a block alterable memory cell of claim 1, wherein said tunnel oxide layer having a thickness of 50-70 angstroms.

4. (withdrawn) The method for manufacturing a block alterable memory cell of claim 1, wherein said screen oxide layer having a thickness of 200-350 angstroms.

5. (currently amended) A block alterable memory cell, comprising:

a substrate layer including an active region having a source implant region, a buried implant region essentially contiguous with said source implant region, a tunnel ~~diode~~ window region ~~within~~ overlaying said buried implant region, ~~an active region, a floating gate transistor region essentially contiguous with said active region,~~ and a drain implant region spaced apart from the buried implant, all in the active region;

a tunnel oxide layer overlaying the tunnel window and a portion of said buried implant region;

a floating gate oxide layer overlaying said ~~floating gate transistor region exclusive of said~~ tunnel ~~diode~~ window region;

a ~~first~~ floating gate layer overlaying said tunnel oxide layer and said floating gate oxide layer;

an interpoly layer having a first region overlaying said ~~first~~ floating gate layer ~~and said active region~~, said interpoly layer having a second region extending continuously from the first region and overlaying an edge of said source implant region to an edge of said drain implant region; and

a ~~second~~ control gate layer extending continuously over said interpoly layer ~~floating gate transistor region and said active region~~, said ~~second~~ control gate layer extending from an edge of said source implant region to an edge of said drain implant region,

whereby the control gate controls a first transistor having said floating gate and simultaneously controls a second adjacent select transistor having said source and drain.

6. (previously presented) The block alterable memory cell of claim 5, wherein said substrate layer is a p-type doped substrate.

7. (previously presented) The block alterable memory cell of claim 5, wherein said source implant region, said drain implant region, and said buried implant region are n-type implants.

8. (currently amended) The block alterable memory cell of claim 5, wherein said ~~first~~ floating gate layer and said ~~second~~ control gate layer are polysilicon.

9. (previously presented) The block alterable memory cell of claim 5, wherein said interpoly layer is a nitride layer.

10. (canceled)

11. (Canceled)

12. (previously presented) The block alterable memory cell of claim 5, wherein said interpoly layer is an ONO layer.

13. (currently amended) A block alterable memory cell, comprising:

a substrate layer including an active region having a source doped region, a buried doped region essentially contiguous with said source doped region, a tunnel ~~diode~~ window region ~~within~~ overlaying said buried doped region, ~~an active region, a floating gate transistor region essentially contiguous with said active region,~~ and a drain doped region, spaced apart from the doped region all in the active region;

a tunnel oxide layer overlaying the tunnel window and at least a portion of said buried doped region;

a floating gate oxide layer overlaying said ~~floating gate transistor region exclusive of said~~ tunnel ~~diode~~ window region;

a ~~first~~ floating gate layer overlaying said tunnel oxide layer and said floating gate oxide layer;

an interpoly layer having a first region overlaying said ~~first~~ floating gate layer ~~and said active region~~, said interpoly layer having a second region extending continuously from the first region overlaying an edge of said source doped region to an edge of said drain doped region; and

a ~~second~~ control gate layer extending continuously over said interpoly layer ~~floating gate transistor region and said active region~~, said ~~second~~ control gate layer extending from an edge of said source doped region to an edge of said drain doped region,

whereby the control gate controls a first transistor having said floating gate and simultaneously controls a second adjacent select transistor having said source and drain.

14. (previously presented) The block alterable memory cell of claim 13, wherein said substrate layer is a p-type doped substrate.

15. (previously presented) The block alterable memory cell of claim 13, wherein said source doped region, said drain doped region, and said buried doped region have n-type dopants.

16. (currently amended) The block alterable memory cell of claim 13, wherein said ~~first~~ floating gate layer and said second layer are polysilicon.

17. (previously presented) The block alterable memory cell of claim 13, wherein said interpoly layer is a nitride layer.

18. (previously presented) The block alterable memory cell of claim 13, wherein said interpoly layer is an ONO layer.

19. (canceled)

20. (canceled)

21. (canceled)

22. (currently amended) An abutting pair of block alterable memory cells, each memory cell comprising:

a substrate layer including an active region having a source implant region, a buried implant region essentially contiguous with said source implant region, a tunnel ~~diode~~ window region ~~within~~ overlaying said buried implant region, ~~an active region, a floating gate transistor region essentially contiguous with said active region,~~ and a drain implant region spaced apart from the buried implant, all in the active region;

a tunnel oxide layer overlaying the tunnel window and a portion of said buried implant region;

a floating gate oxide layer overlaying said ~~floating gate transistor region exclusive of said~~ tunnel ~~diode~~ window region;

a ~~first~~ floating gate layer overlaying said tunnel oxide layer and said floating gate oxide layer;

an ~~end tour poly~~ interpoly layer having a first region overlaying said ~~first~~ floating gate layer ~~and said active region~~, said interpoly layer having a second region extending continuously ~~on~~ from the first region and overlaying an edge of said source implant region to an edge of said drain implant region; and

a ~~second~~ control gate layer extending continuously ~~on~~ over said interpoly layer ~~floating gate transistor region and said active region~~, said ~~second~~ control gate layer extending from an edge of said source implant region to an edge of said drain implant region,

whereby the control gate controls a first transistor having said floating gate and simultaneously controls a second adjacent select transistor having said source and drain.

23. (currently amended) The abutting pair of block alterable memory cells of claim 22, wherein each of said pair of abutting block alterable memory cells ~~is coupled essentially contiguous at said source~~ shares the same buried implant region.

24. (currently amended) An abutting pair of block alterable memory cells, each memory cell comprising:

a substrate layer including an active region having a source doped region, a buried doped region essentially contiguous with said source doped region, a tunnel ~~diode~~ window region ~~within~~ overlaying said buried doped region, ~~an active region, a floating gate transistor region essentially contiguous with said active region,~~ and a drain doped region spaced apart from the buried implant, all in the active region;

a tunnel oxide layer overlaying the tunnel window and a portion of said buried doped region;

a floating gate oxide layer overlaying said ~~floating gate transistor region exclusive of said~~ tunnel ~~diode~~ window region;

a ~~first~~ floating gate layer overlaying said tunnel oxide layer and said floating gate oxide layer;

an ~~end tour poly~~ interpoly layer having a first region overlaying said ~~first~~ floating gate layer ~~and said active region~~, said interpoly layer having a second region extending continuously ~~on~~ from the first region and overlaying an edge of said source doped region to an edge of said drain doped region; and

a ~~second~~ control gate layer extending continuously ~~on~~ over said interpoly layer ~~floating gate transistor region and said active region~~, said ~~second~~ control gate layer extending from an edge of said source doped region to an edge of said drain doped region,

whereby the control gate controls a first transistor having said floating gate and simultaneously controls a second adjacent select transistor having said source and drain.

25. (currently amended) The abutting pair of block alterable memory cells of claim 24, wherein each of said pair of abutting block alterable memory cells shares the same buried ~~is coupled essentially contiguous at said source~~ doped region.

26. (new) A block alterable pair of electrically erasable mirrored cells of a memory array of the type wherein each electrically erasable cell has a word line, a bit line and a select line, the word line and bit line determining the cell address, the select line determining a block operation for a multiplicity of cells, comprising:

a substrate having an active area defined by isolation at the periphery of the cell and having a buried implant in a central region of the active area, a mirrored pair of source implants proximate to the buried implant and a mirrored pair of drain implants at peripheral regions of the active area,

a mirrored pair of floating gates of the type having a tunnel window allowing electrical charge communication with the buried implant through tunnel oxide spaced over the buried implant, the pair of floating gates both having portions overlaying the buried implant, the buried implant being common to both floating gates,

a mirrored pair of control gates each having a first portion in spaced relation above the floating gates and a second portion continuous with the first portion insulatively spaced above the substrate between the sources and drains,

whereby each source acts as a select line, each drain acts as a bit line and each control gate acts as a word line for each memory cell.